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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,115	01/30/2004	Young Hoon Kwark	YOR920030625US1 (163-27)	7189

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EXAMINER	
CHAN, EMILY Y	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/769,115	KWARK, YOUNG HOON	
	Examiner	Art Unit	
	Emily Y. Chan	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-2, 8-10, 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kantz et al US Patent No. 2001/0043078 in view of Kamieniecki et al US Publication No. 2004/0046585.1.

With respect to the claim 1, Kantz et al ('078) disclose a system for measuring circuits on an integrated circuit substrate (see Figs.1-5) as claimed, comprising:

a measurement circuit (Built-in self-test (BIST) 2) formed on the integrated circuit substrate which measures at least one characteristic (functionality of the normal memory cell) of an integrated circuit (chip 1),

The measurement circuit (2) comprising a power transfer device including a power transfer component (voltage detector or current detector 6), which receives energy from a source (energy source 30) where the source (30) does not make physical contact with the integrated circuit substrate (1) to transfer power to the measurement circuit (2) (see page 4, paragraph (0045) "a solar cell 30, which can generate the operating current 1B on the semiconductor chip 1 by optical radiation 31 is fed in **contactlessly**").

Kantz et al ('078) do not disclose that the measurement circuit including components that mirror behavior of the integrated circuit so that process parameters measured for the components to provide information about processing.

Kamieniecki et al ('585) disclose real-time in-line testing of semiconductor wafer during the manufacturing process (see Fig. 1) comprising a light source and a measurement circuit (14). Kamieniecki et al ('585) exclusively teach that their measurement circuit (14) includes components that mirror behavior of the integrated circuit so that process parameters measured for the components to provide information about processing (see Abstract, last two lines " a computer then uses the inducted surface photovoltage to determine various electrical characteristics of the wafer and page 1, paragraph (0007)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to incorporate the teaching of Kamieniecki et al ('585) into Kantz et al ('078)'s measurement circuit (2) for the purpose of having real-time in-line testing of semiconductor wafers during integrated circuit fabrication as disclosed by Kamieniecki et al ('585) (see page 1, paragraph (0001).

With respect to the claim 2, Kantz et al ('078) disclose (see Fig. 4) that the integrated circuit substrate includes a chip (1) formed on a semiconductor wafer (10).

With respect to the claim 10, Kantz et al ('078) disclose a system (see Figs. 1-5) for measuring circuits on an integrated circuit substrate, comprising:

a semiconductor wafer (10) including a plurality of chips (1);

a measurement circuit (2) formed on at least one of the chips, the measurement circuit measures at least one characteristic (functionality of the normal memory cell) of an integrated circuit,

the measurement circuit (2) including a power transfer component which receives energy from a source (energy source 30) where the source does not make physical contact with the semiconductor wafer (10) to transfer power to the measurement circuit (2) (see page 4, paragraph (045) "a solar cell 30, which can generate the operating current 1B on the semiconductor chip 1 by optical radiation 31 is fed in **contactlessly**"); and

Kantz et al ('078) do not disclose a test device including the source (30), which delivers energy to the power transfer component of the measurement circuit when in alignment with power transfer component.

Kamieniecki et al ('585) disclose real-time in-line testing of semiconductor wafer during the manufacturing process (see Fig. 1) comprising a light source and a test device (14). Kamieniecki et al ('585) exclusively teach that their test device (14) including the source (see page 1, paragraph (0007), lines 8-9) which delivers energy to the power transfer component of the measurement circuit when in alignment with power transfer component.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to incorporate the teaching of Kamieniecki et al ('585) into Kantz et al ('078)'s measurement circuit (2) for the purpose of having real-

time in-line testing of semiconductor wafers during integrated circuit fabrication as disclosed by Kamieniecki et al ('585) (see page 1, paragraph (0001).

With respect to the claims 8 and 16, Kantz et al ('078) disclose that the measuring circuit (2) includes a control circuit (6), which conveys measurement information (see page 4, paragraph (0041), last three lines " for the purpose of initiating a function test of account of a detected characteristic voltage sequence or current sequence").

With respect to the claims 9 and 19, Kantz et al ('078) disclose that at least one characteristic includes circuit response (see page 4, paragraph (0039), last five lines).

With respect to the claims 17 and 18, Kantz et al ('078) disclose that the test device includes a thin film dielectric membrane (see Fig. 5A, 12) having the source (30) mounted thereon and includes a probe ring (a support for the thin film dielectric membrane (12)(see page 4, paragraph (0048)).

2. Claims 3 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kantz et al ('078) in view of Kamieniecki et al ('585) as applied to claims 1 and 10 above, and further in view of Fischer et al US Patent No. 6,787,801.

Kantz et al ('078) in view of Kamieniecki et al ('585) do not disclose that the measurement circuit (2) is formed in a kerf area of the chip (1).

Fischer et al ('801) disclose a system for measuring circuits on an integrated circuit substrate comprising a measurement circuit (3) and exclusively teach that the measurement circuit (3) is formed in a kerf area (4) of the chip (1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to incorporate the feature of having measurement circuit formed in the kerf area of the chip as taught by Fischer et al ('801) into Kantz et al ('078) and Kamieniecki et al ('585)and 's system for the expected benefit of providing an improved wafer design for testing integrated circuits on the wafer as disclosed by Fischer et al ('801) (see C0l. 2, lines 45-46).

With the claims 5 and 13, Kamieniecki et al ('585) disclose a photo sensor (92) and a source transfer energy via light (see page 3, paragraph (0040)).

With respect to claims 7 and 15, Kamieniecki et al ('585) disclose that their power transfer device includes a capacitor and the source transfers energy via capacitor coupling.

3. Claims 4 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kantz et al ('078) in view of Kamieniecki et al ('585) as applied to claims 1 and 10 above, and further in view of Cheng et al US Patent No. 6,906,495.

Kantz et al ('078) in view of Kamieniecki et al ('585) do not disclose that the power transfer device (6) includes an inductor coil and the source (30) transfers energy via inductive coupling.

Cheng et al ('495) disclose a system for transferring power and exclusively teach that a power transfer device includes an inductor coil (see Figs 6a-6f) and a source (power supply 760) transfers energy via inductive coupling (see Fig. 5 and Col. 16, lines 37-54).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to incorporate the teaching of transferring energy via inductive coupling as taught by Cheng et al ('495) into Kantz et al ('078) and Kamieniecki et al ('585) 's system for the expected benefit of providing a system for transferring power without requiring direct electrical conductive contacts as disclosed by Cheng et al ('495) (see Col. 4, lines 31-33).

4. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kantz et al ('078) in view of Kamieniecki et al ('585) as applied to claims 1, 5, 10 and 13 above, and further in view of Cook et al US Publication No. 2002/0047722.

Kantz et al ('078) in view of Kamieniecki et al ('585) do not disclose that the source includes a laser.

Cook et al ('722) disclose a contact-less probe of semiconductor wafers (see Figs 1 and 5) and exclusively teach a power transfer component includes photodiode (10) and a source (14) includes a laser (see page 3, paragraph (0046), line 6 " optical power source, such as a laser").

Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to incorporate the teaching of laser as taught by Cook et al ('722) into Kantz et al ('078) and Kamieniecki et al ('585) 's system for the expected benefit of providing a testing devices which do not contact the device under test (DUT) as disclosed by Cook et al ('722) (see page 1, paragraph (0002)).

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kamieniecki US Patent No. 4,827,212 discloses method and apparatus for characterizing a semiconductor using the surface photovoltage effect.

Response to Arguments

Applicant's arguments with respect to claims 1-19 have been considered but are moot in view of the new ground(s) of rejection.

Response to Amendment

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emily Y. Chan whose telephone number is 571-272-1956. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on 571-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC
12/18/05

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